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DESIGN AND MODELLING OF LOW POWER 14NM SINGLE FINSOI-TG-FINFET WITH POWER GATING TECHNIQUE TO LOWER THE POWER DISSIPATION IN STAND-BY MODE

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ABSTRACT. As the IC technology scaled down to lower extent, the device scaling is necessary in which there is an increment in transistor count on die and undesirable short channel effects are included, which disrupts device mechanism. To balance these parameters, non-planar multi-gate devices like Double Gate FinFET (DG-FinFET) and Triple Gate FinFET (TG-FinFET) comes in to existence. But, the power dissipation rises to higher extent. So, there is a need of low power circuit topology to regulate the power dissipation from the devices. Low power design techniques like power gating technique is used to minimize the leakage power during the stand-by mode of operation, which contributes sufficient value to total power dissipation. A power grid circuit is used to minimize supply voltage variations to the circuit. In this paper, we have to modelled a Silicon-on-insulator Triple Gate FinFET (SOI-TG-FinFET), power grid circuit using Verilog-A. The IV characteristics of SOI-TG-FinFET, output waveforms for power grid circuit are verified and a three stage ring oscillator of 2GHZ is implemented as a test circuit in logic block. Results, shows that Power gating technique provides minimal power dissipation of 15% less than non-power gating circuit.

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Key words and phrases. Device scaling, SOI-TG-FinFET, Low power deign technique, Power gating technique, power grid circuit, Verilog-A.

1. INTRODUCTION

Scaling of transistor to the lower technology node in Complementary metal oxide semiconductor (CMOS) logic design, leads to occurrence of undesirable short channel effects (SCE's) and also gradually increase in leakage power. So there is a need of newer device architecture to control these SCE's and better topology to reduce the leakage power. In conventional Metal oxide semiconductor field effect transistor (MOSFET), gate terminal is responsible for channel formation and controls the flow of charge carriers through the channel , as the channel length reduces the behaviour of the device is changed and those disruptions are defined by phenomenon's called Drain induced barrier lowering, velocity saturation, hot carrier injection, surface scattering[1]. In order to minimize these effects, improved gate controlling mechanism by multiple gates is used. Multi-gate controlling can be implemented using newer technology devices like silicon-on-insulator-MOSFET (SOI-MOSFET) and variable gate FINFET's. SOI-MOSFET is differentiated from MOSFET by placing buried oxide an insulator above the silicon substrate, these results in reduction of junction virtual capacitance, unwanted latch-up formation and leakage power [2].There are two types of SOI-MOSFET's, those are Fully depleted SOI-MOSFET (FD-SOI-MOSFET) and Partially depleted SOI-MOSFET (PD-SOI-MOSFET). There are some disadvantages of SOI-MOSFET are self-heating and difficultly to manufacture thin silicon body.

To withstand these effects, three dimensional non-planar devices like multi gate FinFET's are used .The word Fin is due to the non-planar elevated channel of the device which looks like a fish fins, there results that gate controlling can be done on all sides of the channel. There are different types of FinFET architectures Double gate FinFET (DG-FinFET), Triple gate FinFET (TG-FinFET). A Three dimensional multi gate FinFET is as shown in figure 1 [3], irrespective of its non-planar nature this device shows same characteristics as conventional MOSFET. FinFET controls SCE'S by electrical coupling of gates and increases output drive currents by increasing number of fins in the device structure [4]. The advantages of FinFET are higher speed, lower leakage, low power consumption which are used in low power circuit design, in addition to this there are some disadvantages like quantum effects, corner effects, width quantization, complex fabrication process [5]. In digital circuit design, transistor acts

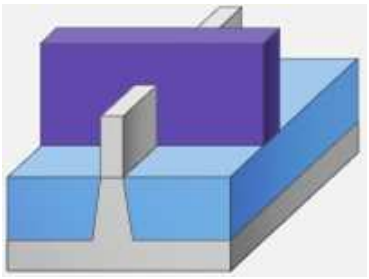

FIGURE 1. 3D FinFET structure.

as a switch. So, number of transistors are used to implement the logic. At the initial phase of IC designing reliability, area, cost are primary concern, but as the device scaling and transistor density on die increases gradually results in consideration of power, performance and area constraints. As the density of transistors increases on die, power density increases gradually. The power dissipation can be formulated as

$$P = C * F * V_{dd}^2 \tag{1.1}$$

From (1.1), power dissipation depends on load capacitance (C), operating frequency (f) of the circuit and supply voltage (V_{dd}). So, there is a need of leakage power absorption, there by the concept of low power design is evolved. In low power circuit design, different topologies are implemented with less number of transistors without deviation in circuit logic. There are different sources of power dissipation, those are static power dissipation, dynamic power dissipation and leakage power dissipation. To reduce these dissipation low power techniques like Multi threshold CMOS, Power gating, clock gating, body biasing and reduction in supply voltage are used. Out of those power minimization techniques, we use power gating technique to acquire power efficiency factor, irrespective of increase in area occupancy factor [6].

The advantages of low power techniques are reduction in leakage current, power dissipation, whereas disadvantages are state retention problem, increase in delay and area of the circuit. Low power circuits are used primarily for portable or battery operated device applications like pocket calculators, mobile phones, laptops [7]. The new device architecture like multi gate FinFET's are replaced in place of MOSFET by different tech fabrication units. The paper is organized in following sections, FinFET modelling is discussed in section II, power

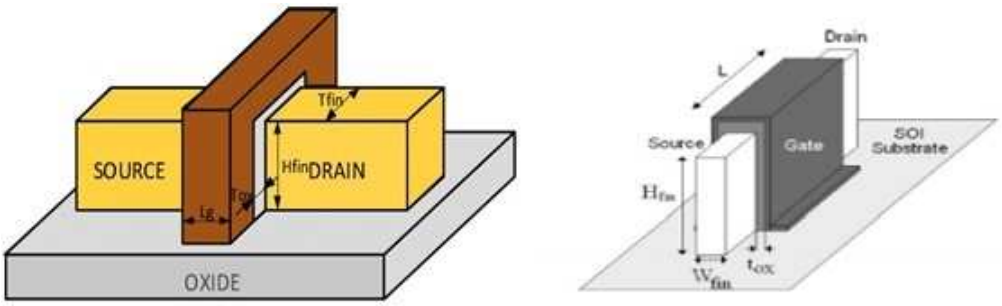

FIGURE 2. schematic view of SOI-TG-FinFET.

grid circuit is discussed in section III, power gating technique is explained in section IV, Results are discussed in section V and conclusion in section VI.Design and Modelling of Low power 14nm single FinSOI-TG-FinFET with Power Gating Technique 3 to Lower the Power Dissipation in Stand-by mode

See also [8] and [10].

2. FINFET MODELLING

In order to minimize the undesirable SCE's, we have to model a 14nm SOI-TG-FinFET for the realization of the circuit. In SOI-TG-FinFET, Fin is enclosed by three gates provides better controlling over the channel by the electrical coupling of three gates mechanism. The SOI-TG-FinFET is shown in figure 2[5] and the symbols of n-type and p-type SOI-TG-FinFET is shown in Figure3, which consists of gate, source, drain and reference terminals. Where reference terminal is treated as a body terminal like in Independent gate FinFET (IG-FinFET). The intermediate buried oxide layer prevents the latch-up formation, reduces parasitic capacitance results in reduction of leakage current and power dissipation with penalty in thickness of the device. The effective width of the fin (W_{eff}) can be formulated in terms of height of the fin (H_{fin}) and silicon substrate thickness t_{si} in (2.1).

$$W_{eff} = 2 * H_{fin} + t_{si}. \tag{2.1}$$

A capacitance based compact model of TG-FinFET can be described in Verilog-A script. Compact modelling refers to the development of device models during IC designing phase, results in reduction of cost and manufacturing time. The capacitance model of TG-FinFET defines the device model in terms of charges at

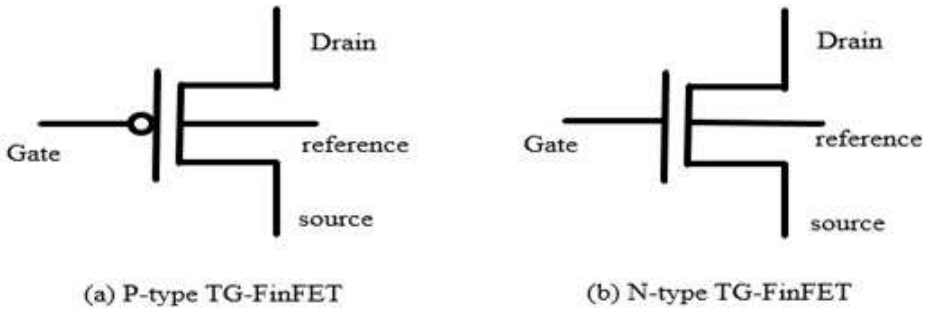

FIGURE 3. TG-FinFET symbols.

source, drain and gate terminals [9]. As shown from figure 2, the gate terminal is wrapped around the outer portions of the fin, in this compact model the three gate terminals are consolidated and thereby considered as a single gate terminal. The current equations derived from the capacitance device Model is as follows

$$I_D = 2W\mu_{eff}\frac{\epsilon_{ox}}{t_{ox}}(2V_{th})^2\left[\frac{(q_{is}-q_{id})}{L}\right].$$

The above current equation is for below sub-threshold region. The current equation of TG-FinFET for above sub-threshold region is as shown below.

$$I_D = 2W\mu_{eff}\frac{\epsilon_{ox}}{t_{ox}}(2V_{th})^2\left[\frac{1}{2}\frac{(q_{is}^2-q_{id}^2)}{L-\triangle L}\right].$$

The necessary equations along with device parameters are described in the form of voltage and current relationship in Verilog-A script. The device model can be treated as a black box, with inputs and outputs are displayed and it is simulated in commercial simulator to verify the characteristics of the device model. The device model parameters are defines in Table-1.

3. POWER GRID

In an Integrated circuit(IC), transistors are connected to the supply voltage and ground rails. A Power grid circuit, which is a power distribution network is placed between supply rails and logic circuit .This because the current flow in the circuit depends on the transient inputs that are given to the transistor controlling terminals (Gate). So, there is a requirement of transient power distribution network next to supply rails [11] with variation in supply voltage. But these variations in voltage contribute delay, clock skew and occurrence of Meta

TABLE 1. SOI-TG-FinFET parameters

S. no	Parameter	value
1.	Channel length (L)	20nm
2.	Width of the Fin(W)	10nm
3.	Height of the Fin (H)	40nm
4.	Thick oxide thickness (t_{ox})	1nm
5.	Supply voltage	0.7v
6.	Intrinsic carrier concentration (n_i)	1.45e10 cm^{-3}
7.	Thick oxide permittivity ($\in_{ox}$)	3.54e-13 C/Vcm
8.	Donor concentration (N_d)	1e20 cm^{-3}
9.	Acceptor concentration (N_a)	1.45e10 cm^{-3}

stable transitions. In deep submicron process, transistor count increases there by computation becomes more complex results in more power distribution. These high power and clock frequency circuits with lower supply voltage contribute to noise with time varied currents. In order to fix these voltage variations, a decoupling capacitance (decap) is used. The power distribution network consists of resistances and capacitances, which are arranged in following fashion as shown in figure 4 [12]. The topology of logic circuit with power grid circuit is as follows [Figure 5].

4. POWER GATING TECHNIQUE

The radiated energy from the circuit can be described as power dissipation in the IC's, which is measured in watts and the three major sources of power dissipation are short circuit power dissipation, dynamic power dissipation and leakage power dissipation. The short circuit power dissipation is due to simultaneous triggering of MOS transistors, dynamic power dissipation is due to continuous charging and discharging of capacitances associated at every node of the

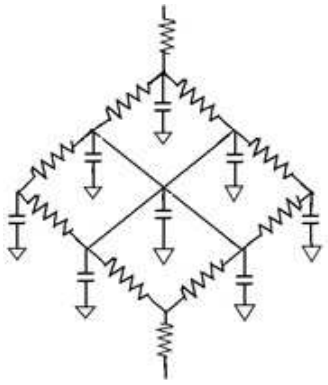

FIGURE 4. power grid circuit.

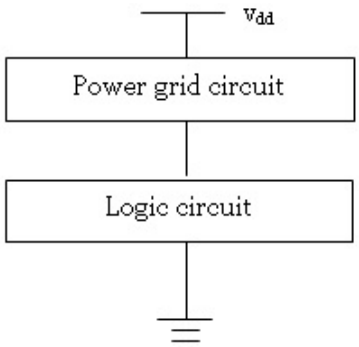

FIGURE 5. circuit topology with power grid circuit.

circuit whereas leakage power dissipation is due to static devices in the circuit. As the leakage power dissipation increases, there is a reduction in sub-threshold slope. Therefore, the total power dissipation can be formulated as algebraic sum of short circuit, dynamic, leakage power dissipations [6].

$$P_{total} = P_{shortcircuit} + P_{dynamic} + P_{leakage}. \tag{4.1}$$

From (4.1), leakage power dissipation contributes sufficient amount power dissipation. So, to reduce it, we use low power design topology circuit to minimize it. For this implementation, we have to use power gating technique, which shuts off the logic circuit during stand-by mode. The topology consists of high threshold voltage Field effect transistors (FET's) $(highV_{th})$ and low threshold voltage FET's $(lowV_{th})$ as a sleep transistors or header switches. During ON-state or dynamic mode, sleep transistor is in ON state, provides supply voltage to logic

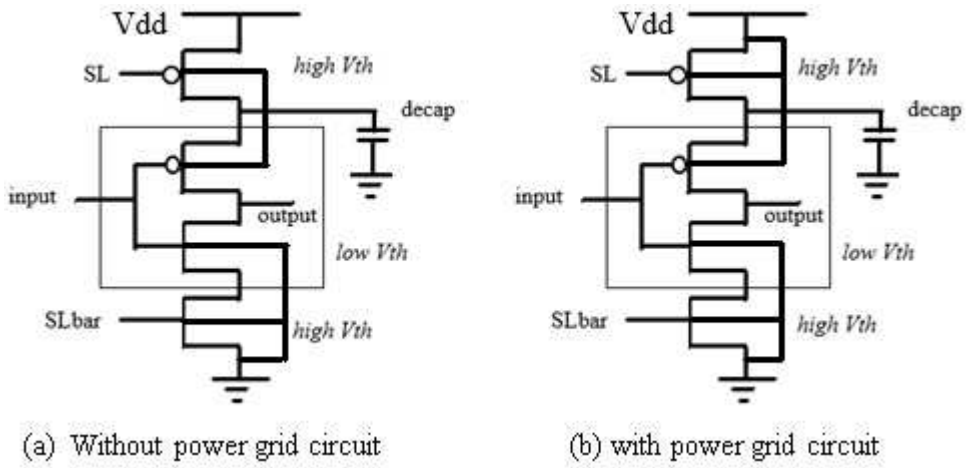

FIGURE 6. power gating topology forSOI-TG-FINFET inverter.

block whereas in OFF state, sleep transistor is turned OFF, thereby blocking of logic circuit from supply voltage (V_{dd}) and reduces the dissipation of leakage power from stand by transistors and results in reduction of total power dissipation [13]. The power gating phenomenon for CMOS inverter with and without power grid can be described as shown in figure 6a, 6b. The topology of logic circuit with power grid circuit is as follows [Figure 5]. The box in figure 6a, 6b is a logic block, sleep transistors are triggered by SL and SLbar inputs. As the sleep transistors are triggered dynamically, considerable power supply currents are drawn in a short time period and produces fluctuations in power distribution network and this phenomenon is termed as power gating noise (PGN).To omit this effect, we insert decap as a compensating agent for PGN and switching noise. Decap can be realized by either on-chip non-switching capacitors, thin-oxide capacitors. But, due to the essence of sleep FET's and decap leakage currents are added and leads to more power dissipation. So, leakage power dissipation is the summation of decap leakage and gate leakage is shown in (4.2).

$$P_{leakage} = P_{logicgates} + P_{decap}. \tag{4.2}$$

The advantages of power gating technique are stand-by leakage power dissipation and quiescent current I_{ddq} testing. Whereas noise, performance and area penalties are added.

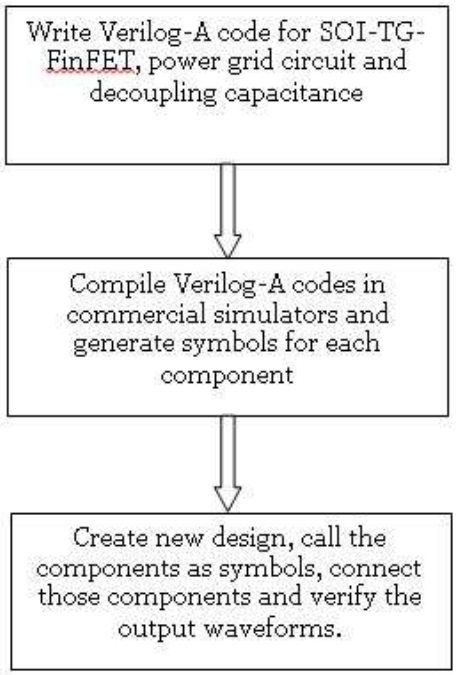

FIGURE 7. flow chart for implementation of power gating mechanism in commercial simulator.

5. RESULTS AND DISCUSSIONS

The flow chart for the execution and designing of power gating mechanism using modeled SOI-TG-FinFET, power distribution network and decap is as shown in figure 7.

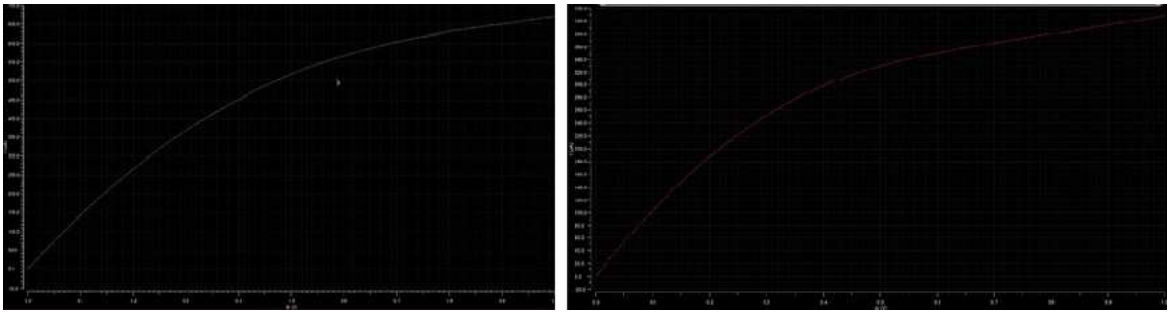

FIGURE 8. IV Characteristics of SOI-TG-FinFET.

a) The IV characteristics of both N-type and P-type SOI-TG-FinFET implemented in commercial simulators is as shown in figure 8.

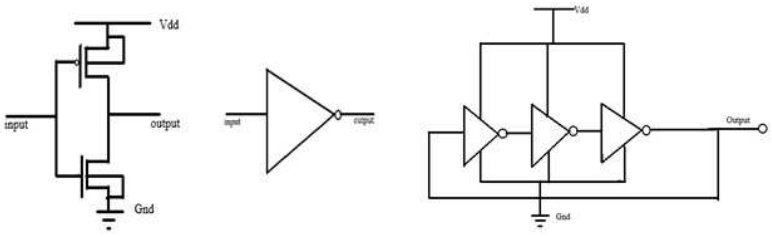

FIGURE 9. Three stage Ring oscillator using inverter.

b) Ring oscillator implementation using power gating technique:-

A Ring oscillator, which is used as a test circuit to demonstrate the power gating phenomenon. The frequencies of oscillations are generated by cascading of odd number of SOI-TG-FinFET inverters and also by feedback mechanism which is shown in figure 9.

The SOI-TG-FinFET inverter, which is used as a delay element. As the number of delay elements are increased results in reduction of frequency of oscillations which can be formulated as shown in (5.1).

$$F = \frac{1}{(2 * t_{pd} * n)}, \tag{5.1}$$

where n is number of stages of inverters, t_{pd} is propagation delay and the factor 2 is one for high to low transition and another for low to high transition of nt_{pd} [14]. The parameters associated with this implementation are shown in table 2. The proposed design of power gating technique with modeled TG-FinFET and power grid circuit is shown in shown in figure 10.

6. CONCLUSION

SOI-TG-FinFET, power grid circuit modeling is done by using Verilog-A. Power gating technique is implemented using modeled devices and circuits, IV characteristics of SOI-TG-FinFET and output waveforms of power gating technique are verified by using commercial simulator. A three stage ring oscillator, which generates 2GHZ oscillating frequency, is used in logic block of power gating topology by using modeled SOI-TG-FinFET and results shows that power dissipation of the power gating circuit is 15% less than non-power gating circuit.

TABLE 2. parameters of the circuit.

S. No	Parameters	Values
1.	Supply voltage (V_{dd})	0.7v
2.	Number of oscillator stages(n)	3
3.	Frequency	2GHZ
4.	Resistance in power grid circuit	6mΩ
5.	Capacitance in power grid circuit	0.2fF
6.	Decoupling capacitance (decap)	100fF

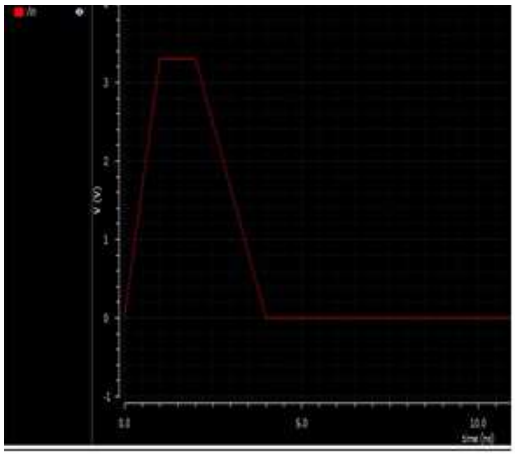

Figure11: piecewise input.

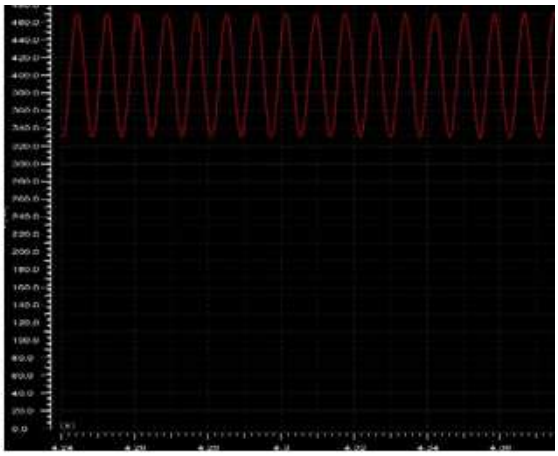

Figure12: Ring oscillator output.

TABLE 3. power dissipation of power gating circuit and non-power gating circuit.

S. No	Parameter	Value
1.	Power dissipation of non-power gating circuit	7.7μwatts
2.	Power dissipation of non-power gating circuit	6.5μwatts

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