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HARMONIC ANALYSIS OF REDUCED DEVICE COUNT MULTILEVEL CONVERTER

B. LALITHA[1], K. LAKSHMI, G. RAMYA, R. SAMPATHKUMAR,
AND T. GULAM MOHAMMED MOINUDDEEN

ABSTRACT. The dc-ac converter especially multilevel inverters become an option for various applications present trends. Among various topology structure H bridge Inverter which comprises of a progression ofH connect section along seperate direct current sources is connected to create stepped voltage level, and also it has lower switching loss contrasted with different topologies. With increasing the number of level in output the switching device requirement is also increased which results in complex topology structure and control. To report this issue a conventional structure has been presented in this paper which results in increased efficiency and losses. Compartive analysis based on harmonic distortion is carried out in this research paper on convetional MLI and reduced switch count MLI. The proposed MLI structure requires only 24 switches compared to conventional topology which requires twice that of proposed topology. The comparison result also carried out based on harmonic distortion and device count.

1. INTRODUCTION

Due to increased application on higher voltage multilevel inverter is considered as an alternative on basic inverter topology [1]. It produces the necessary output with various DC sources connected H bridge unit. It produces stepped output waveform. MLI has advantages such as reduced circuit and dv/dt stress,

[1]*corresponding author*

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Key words and phrases. Multilevel inverter, PWM, Switch count, THD.

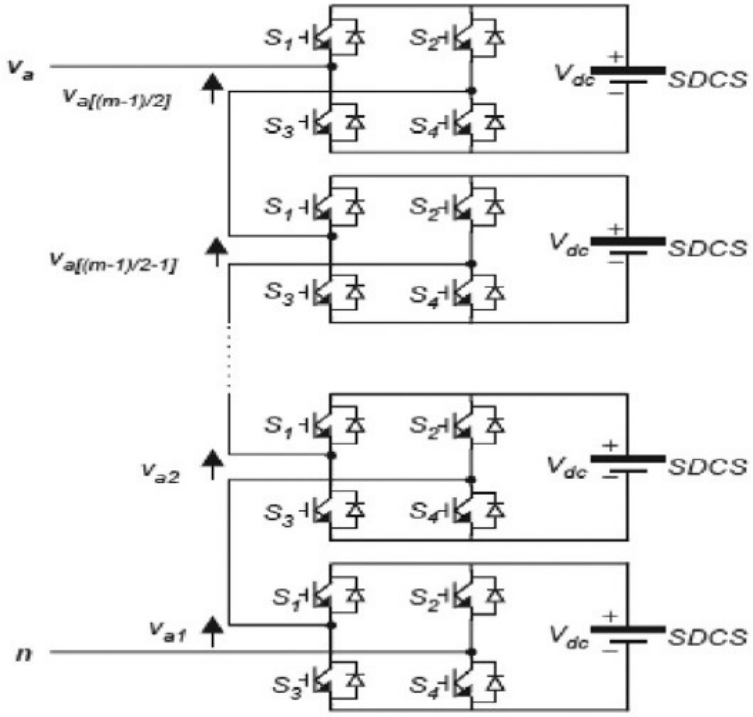

FIGURE 1. Schematic circuit of conventional MLI topology

low filter, reduced harmonics which is suitable for Photovoltaic based system. Various PWM techniques for MLI is analysed in various literature [2]. The various topology has been discussed [3]. Among all topologies CHBMLI is preferred and depicted in Fig. 1. The topology comprises of individual H bridge section. When number of level is increased it produces better performance with the drawback of increased device count. To overcome this, the proposed topology is introduced and discussed in this paper. Various reduced count MLI is discussed in many research work [4].

The Proposed MLI structures comprise of bidirectionals power devices with less number if other deivce count reported in the literature [5-8].In this paper, the comparative stiudy of conventional and proposed MLI is analyzed. The operation of power switches is shown in Table 1.

The output is generated by voltage conversion and H bridge generated stepped output om further processing. The switches S5 and S6 are used in (+)ve half cycle and S7 and S8 are processed on (-)ve half cycle. The proposed topology is

TABLE 1. Switching sequence of proposed MLI

Modes	Switching Sequence		Output
	ON	OFF	
1	S5, S6	S7, S8	$+1V_{dc}$
2	S5, S6	S7, S8	$+2V_{dc}$
3	S5, S6	S7, S8	$+3V_{dc}$
4	S5, S6	S7, S8	$+4V_{dc}$
5	S5, S7	S6, S8	0
6	S7, S8	S5, S6	$-1V_{dc}$
7	S7, S8	S5, S6	$-2V_{dc}$
8	S7, S8	S5, S6	$-3V_{dc}$
9	S7, S8	S5, S6	$-4V_{dc}$

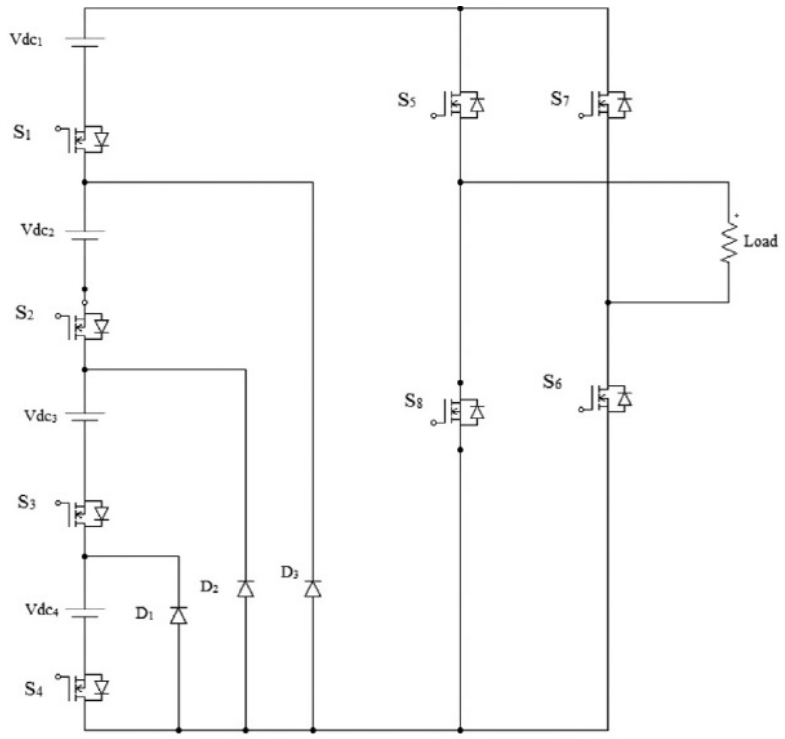

FIGURE 2. Schematic circuit of proposed MLI topology

shown in Fig. 2. The N_{switch} is number of input sources and given by,

$$N_{level} = (2 * S) + 1. \tag{1.1}$$

when S = 4, it results in nine level output. The switch count is determined by the below equation,

$$M_{switch} = S + 4 \tag{1.2}$$

If S = 4, M_{switch} = 8.

$$M_{switch} = S - 1 \tag{1.3}$$

If S = 4, M_{switch} = 3.

2. Working Principle of Proposed Topology

Fig. 3 represents the operation modes of proposed topology. There are five modes of operation based on Table 1.

Mode 1. It is operated by switching ON S1, and first level output voltage $+1V_{dc}$ level is generated as depicted in Fig. 3(a).

Mode 2. It is operated by switching ON S1 and S2 resulting in $+2V_{dc}$ level as in Fig. 3 (b).

Mode 3. It generates the output of $+3V_{dc}$ by switching on first three switches as in Fig. 3(c).

Mode 4. It generates $+4V_{dc}$ output voltage by switching on S1 to S4 as shown in Fig. 3(d).

Mode 5. It is operated by operating S5 and S7 which results if zero output level. Similarly, S7 and S8 is turned on for negative half cycle. From [9-10], the fourier expansion of waveform is given by,

$$f(\omega t) = \sum_{n=1,15,..}^{\infty} \frac{4}{n\pi} \left(\sum_{y=1}^{x} A_y cos(\alpha_y n) \right) sin(n\omega t). \tag{2.1}$$

The x firing anlge is expressed by,

$$x = \frac{N-1}{2}. \tag{2.2}$$

N is harmonic component THD can be calculated by the formula as represented in Eq. 2.3 [9].

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{rms}^2}}{V_{1rms}} \times 100. \tag{2.3}$$

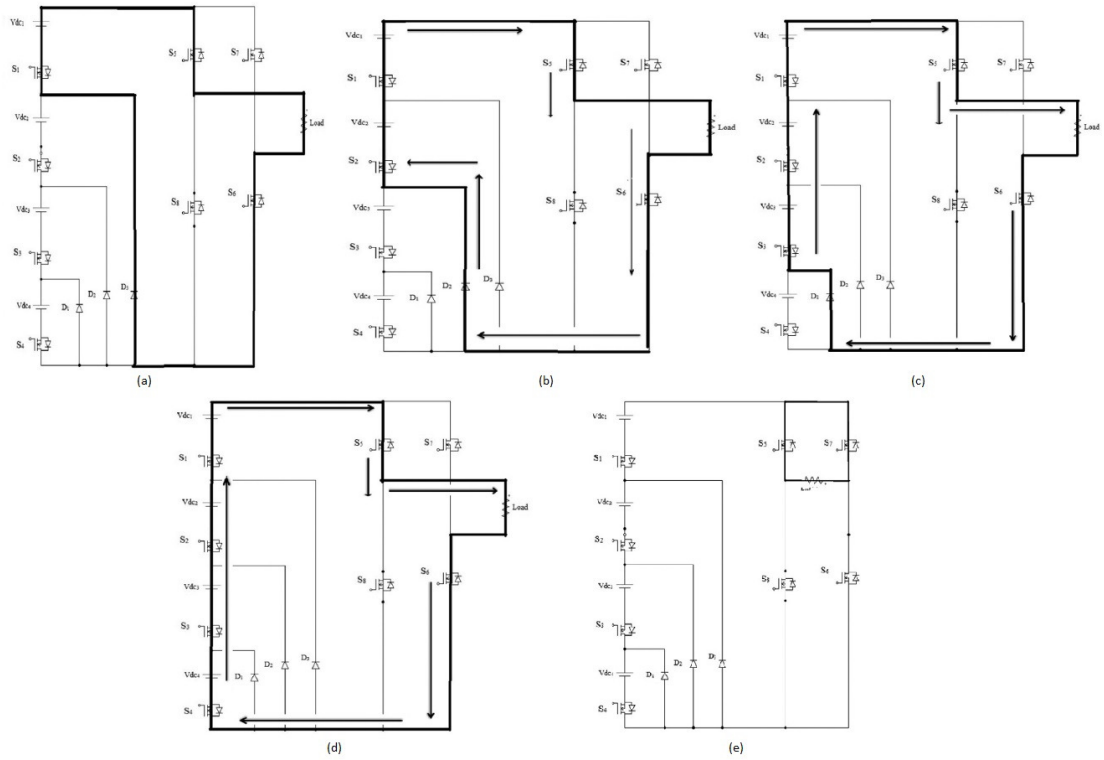

FIGURE 3. Modes of Operation; (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4,(e) Mode 5

Various PWM techniques has been carried out to the proposed inverter topology. In this paper POD and APOD PWM techniques are considered and implemented. For 9 level output voltage 8 carrier signals are required (i.e.(N-1)). The modulation index can be calculated by,

$$MI = \frac{2A_m}{(N-1)A_c}. \tag{2.4}$$

In Phase Opposition Disposition (POD) PWM technique the carrier signals are in phase to each other above and below the zero level as depicted in Fig. 4.

Alternate phase opposition disposition PWM method (APOD PWM). In APOD PWM method the carrier signals are 180 degree out of phase with each other as depicted in Fig. 5.

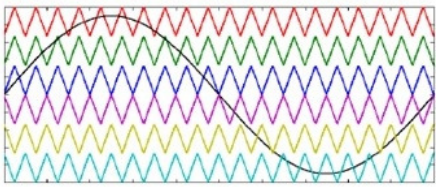

FIGURE 4. Carrier signal of POD PWM

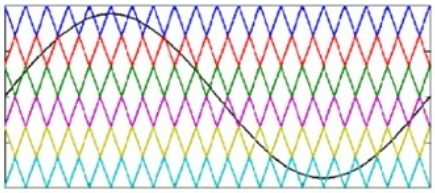

FIGURE 5. Carrier signal of APOD PWM

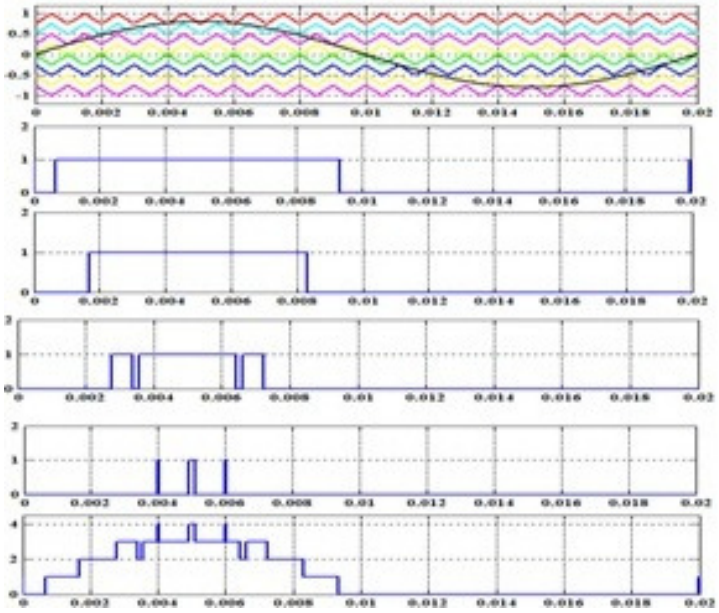

FIGURE 6. Phase opposition disposition strategy

3. SIMULATION RESULTS

Conventional MLI and proposed topology with APOD and POD PWM technique has been simulated using MatLab and the results are presented. The switching pattern of POD PWM techniaue is shown in Fig. 6. The switching

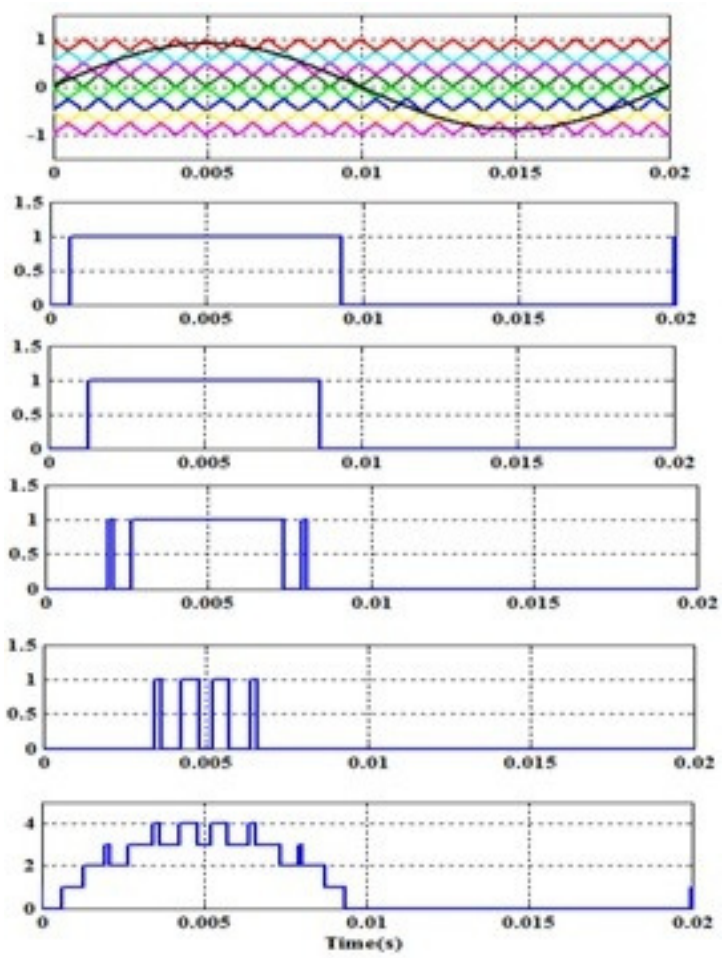

FIGURE 7. Alternate phase opposition disposition strategy

pattern and gating pulase for proposed MLI topology is shown in Fig. 7 using APOD PWM technique.

The nine level output voltage of conventional MLI using APOD and POD PWM technique is shown in Fig. 8.

The nine level output voltage of proposed MLI using APOD and POD PWM technique is shown in Fig. 9.

The THD percentage of conventional MLI using APOD and POD PWM technique is shown in Fig. 10.

The THD percentage of proposed MLI using APOD and POD PWM technique is shown in Fig. 11.

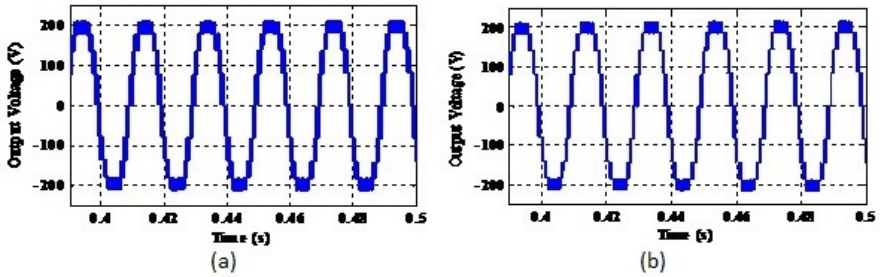

FIGURE 8. Nine level output voltage of conventional MLI; (a) APOD PWM, (b) POD PWM

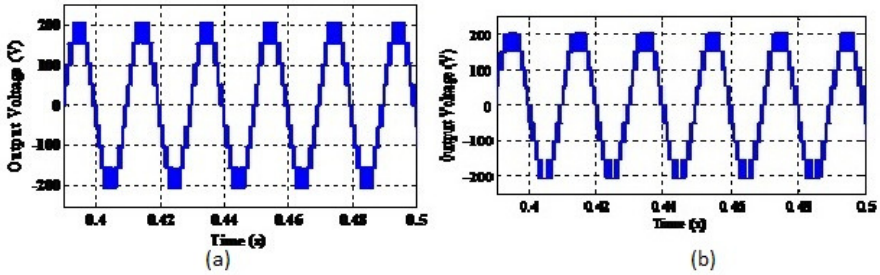

FIGURE 9. Nine level output voltage of proposed MLI; (a) APOD PWM, (b) POD PWM

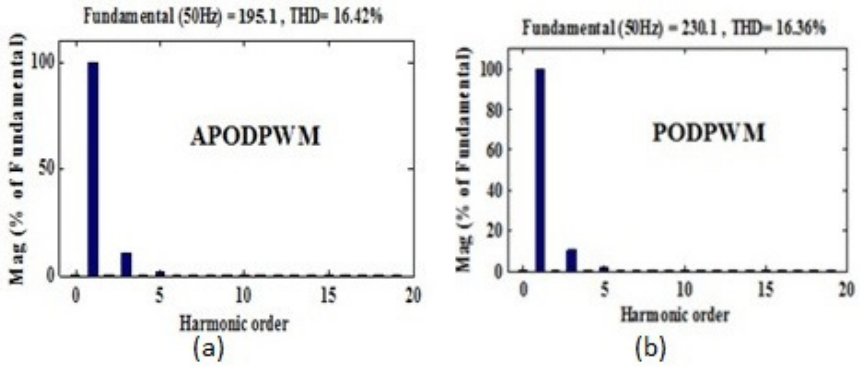

FIGURE 10. THD of conventional MLI; (a) APOD PWM, (b) POD PWM

Table 2 shows the analysis THD percentage of conventional and proposed MLI using APOD and POD PWM technique. The graphical representation of THD analysis is shown in Fig. 12. It is inferred from the analysis that in proposed

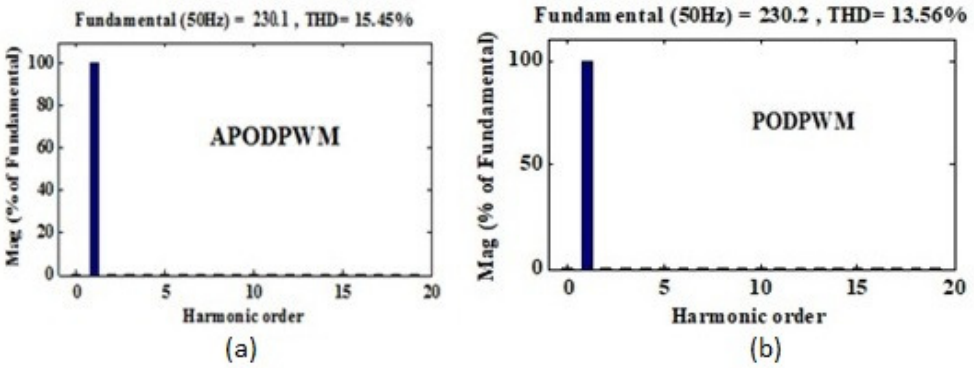

FIGURE 11. THD of proposed MLI; (a) APOD PWM, (b) POD PWM

TABLE 2. Switching sequence of proposed MLI

Parameters	Conventional MLI		Proposed MLI	
PWM	POD	APOD	POD	APOD
THD	16.36	16.42	13.56	15.45

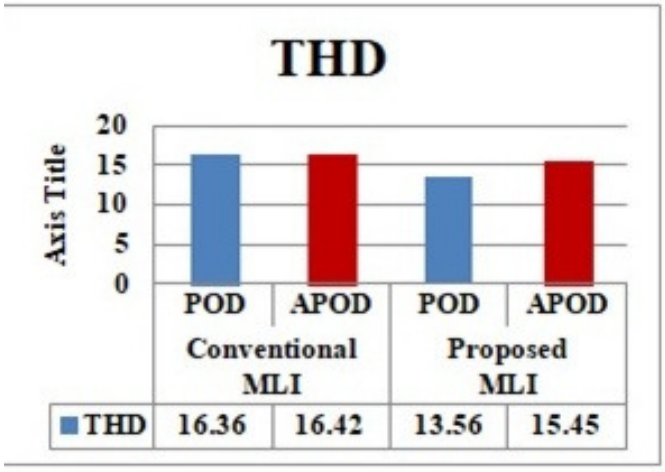

FIGURE 12. THD analysis chart of conventional and proposed MLI with APOD and POD technique

MLI topology it has less THD percentage of about 13.56 when using POD PWM technique compared to others.

4. Conclusion

It is inferred from the obtained results such that the proposed topology is superior over conventional one based on performance and device count. The conventional MLI uses $2(m-1)$ switch count in which for 9 level output voltage we require 16 power switches. In case of proposed MLI topology only 8 power switches which could be concluded that only half count of switch is utilized. It results in less component requirement and low switching losses. Based on THD the proposed MLI using POD PWM technique has less THD percentage compared to APOD PWM technique. Hence it is inferred that POD PWM technique has better harmonic performance.

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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
KPR INSTITUTE OF ENGINEERING AND TECHNOLOGY
COIMBATORE, TAMIL NADU, INDIA
Email address: blalithaphd@gmail.com

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
SRI KRISHNA COLLEGE OF TECHNOLOGY
COIMBATORE, TAMIL NADU, INDIA
Email address: blalithaphd@gmail.com

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
SAVEETHA SCHOOL OF ENGIEERING
CHENNAI, TAMIL NADU, INDIA
Email address: ramyag.sse@saveetha.com

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
KPR INSTITUTE OF ENGINEERING AND TECHNOLOGY
COIMBATORE, TAMIL NADU, INDIA
Email address: blalithaphd@gmail.com

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
DE SMET ENGINEERS AND CONTRACTORS INDIA PVT. LTD.
CHENNAI, TAMIL NADU, INDIA
Email address: blalithaphd@gmail.com